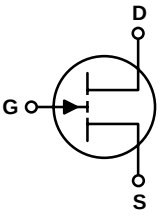
INN030FQ015A

1. General Description

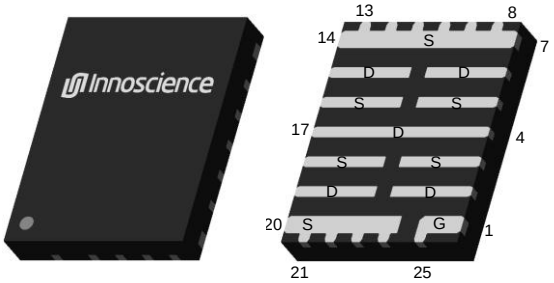
GaN-on-Silicon enhancement mode high-electron-mobility-transistor (HEMT) in FCQFN with 5 mm x 4 mm package size.

2. Features



- GaN-on-Silicon E-mode HEMT technology
- Very low gate charge
- Ultra-low on resistance
- Zero reverse recovery charge

3. Applications



- High frequency DC-DC converter
- Battery charger
- Battery management system
- Notebook
- Industry

4. Key Performance Parameters

Table 1 Key performance parameters at T_J = 25 °C

Parameter	Value	Unit
$V_{DS,max}$	30	V
$R_{DS(on),max}$ @ V_{GS} = 5 V	1.5	mΩ
$Q_{G,typ}$ @ V_{DS} = 15V	22.8	nC
$I_{DS,Pulse}$	300	A
Q_{OSS} @ V_{DS} = 15V	43	nC

5. Pin Information

Table 2 Pin information

Pin	Pin description	Pin function
1, 25	Gate	Driver Gate
3, 5, 7-14, 16, 18, 20-24	Source	Source
2, 4, 6, 15, 17, 19	Drain	Power Drain

Table 3 Ordering information

Type/Ordering Code	Package	Product Code
INN030FQ015A	FCQFN 5mm x 4mm	C06

Table of Contents

6. Maximum Ratings

at T_J = 25 °C unless otherwise specified.

Continuous application of maximum ratings can deteriorate transistor lifetime. For further information, contact Innoscience sales office.

Table 4 Maximum ratings

SYMBOL	PARAMETER	MAX	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	30	V
I_D	Continuous Current	60	A
	Pulsed (25˚C, T_{Pulse} = 300 µs)	300	A
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	V
P_{tot}	Power dissipation (T_B = 25°C)	85	W
T_J	Operating Temperature	-40 to 150	˚C
T_{STG}	Storage Temperature	-40 to 150	˚C

7. Thermal Characteristics

Table 5 Thermal characteristics

SYMBOL	PARAMETER	TYP	UNIT	Note/Test Condition
$R_{\theta JC}$	Thermal Resistance, Junction to Case	12.4	˚C/W	
$R_{\theta JB}$	Thermal Resistance, Junction to Board	1.5	˚C/W	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient [1]	54.5	˚C/W	
T_{sold}	Maximum Reflow Soldering Temperature	260	˚C	MSL3

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

8. Electric Characteristics

at T_J = 25 °C, unless specified otherwise

Table 6 Static characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
BV_{DSS}	Drain-to-Source Voltage	30	-	-	V	V_{GS} = 0 V, I_D = 50 μA
I_{DSS}	Drain Source Leakage	-	10	100	μA	V_{GS} = 0 V, V_{DS} = 24 V
	Drain Source Leakage (125 °C)	-	100	1000	μA	V_{GS} = 0 V, V_{DS} = 24 V
I_{GSS}	Gate-to-Source Forward Leakage	-	6	60	μA	V_{GS} = 5 V
	Gate-to-Source Forward Leakage (125 °C)	-	60	600	μA	V_{GS} = 5 V
	Gate-to-Source Reverse Leakage	-	30	300	μA	V_{GS} = -4 V
$V_{GS(TH)}$	Gate Threshold Voltage	0.9	-	2.1	V	V_{DS} = V_{GS}, I_D = 5 mA
$R_{DS(on)}$	Drain-Source On-state Resistance	-	1.2	1.5	mΩ	V_{GS} = 5 V, I_D = 15 A
V_{SD}	Source-Drain Forward Voltage	-	1.65	-	V	I_S = 0.5 A, V_{GS} = 0 V

Table 7 Dynamic characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
C_{ISS}	Input Capacitance	-	3.4	-	nF	V_{GS} = 0 V, V_{DS} = 15 V
C_{OSS}	Output Capacitance	-	1.8	-		V_{GS} = 0 V, V_{DS} = 15 V
C_{RSS}	Reverse Transfer Capacitance	-	0.1	-		V_{GS} = 0 V, V_{DS} = 15 V
$C_{OSS(ER)}$	Energy Related C_{OSS}	-	2.5	-		V_{GS} = 0 V, V_{DS} = 0 V to 15 V
$C_{OSS(TR)}$	Time Related C_{OSS}	-	2.8	-		V_{GS} = 0 V, V_{DS} = 0 V to 15 V
R_G	Gate resistance	-	1.6	-	Ω	f = 1 MHz
Q_G	Total Gate Charge	-	22.8	-	nC	V_{GS} = 5 V, V_{DS} = 15 V, I_D=15 A
Q_{GS}	Gate to Source Charge	-	5.5	-		V_{DS} = 15 V, I_D=15 A
Q_{GD}	Gate to Drain Charge	-	3.2	-		V_{DS} = 15 V, I_D=15 A
$Q_{G(TH)}$	Gate Charge at Threshold	-	3.8	-		V_{DS} = 15 V, I_D=15 A
Q_{OSS}	Output Charge	-	43	-		V_{GS} = 0 V, V_{DS} = 15 V

9. Electric Characteristics Diagrams

at T_J = 25 °C, unless specified otherwise

Figure 1 Typical Output Characteristics (T_J=25°C)

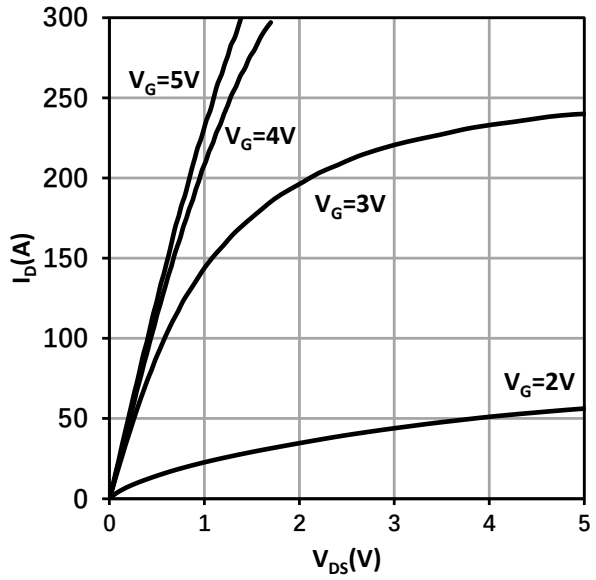


Figure 2 Typical Output Characteristics (T_J=125°C)

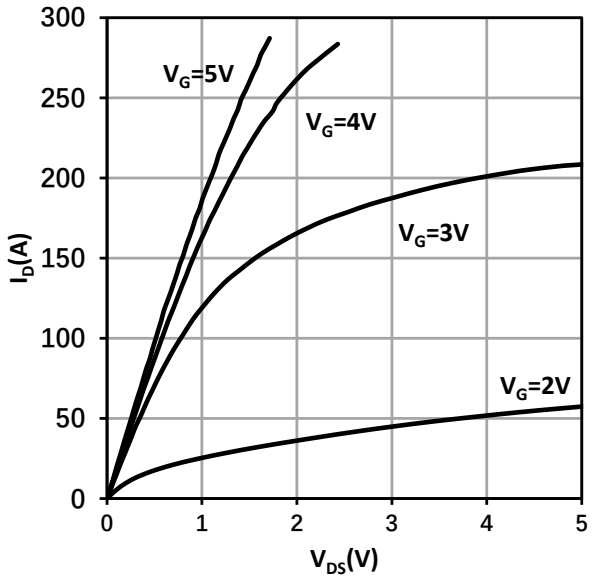


Figure 3 Typical On-state Resistance (T_J=25°C)

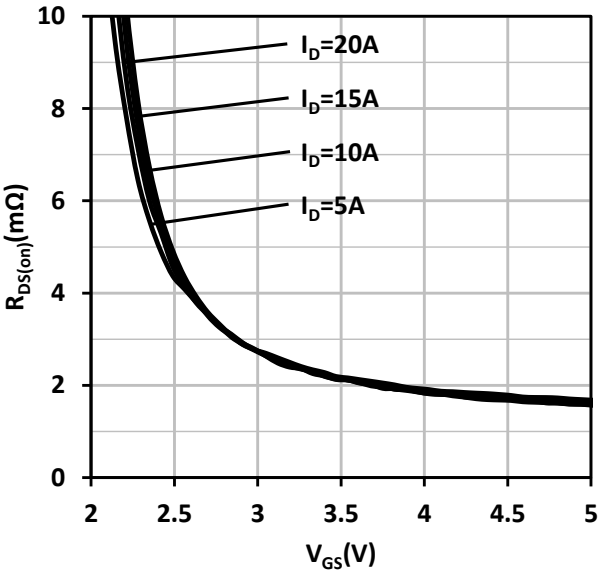


Figure 4 Typical On-state Resistance (T_J=125°C)

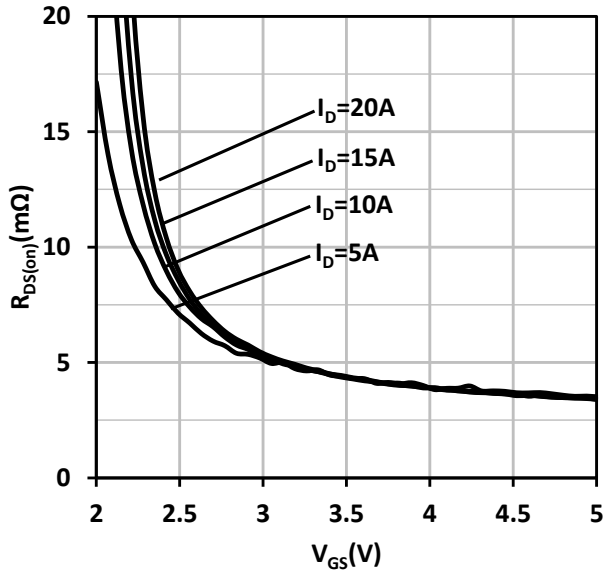


Figure 5 Normalized On-State Resistance vs. Temp.

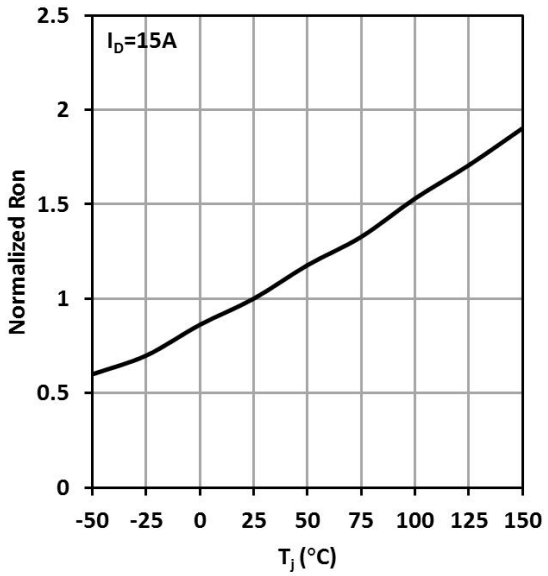


Figure 6 Typical Transfer Characteristics

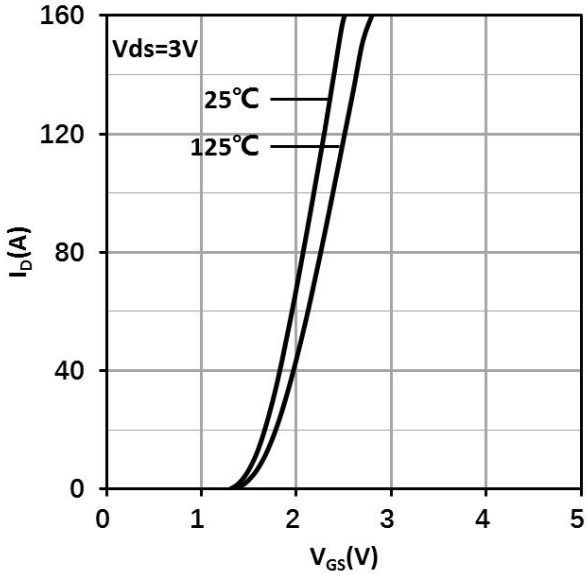


Figure 7 Typical Reverse Characteristics
($V_{GS}\leqslant 0, T_J$=25°C)

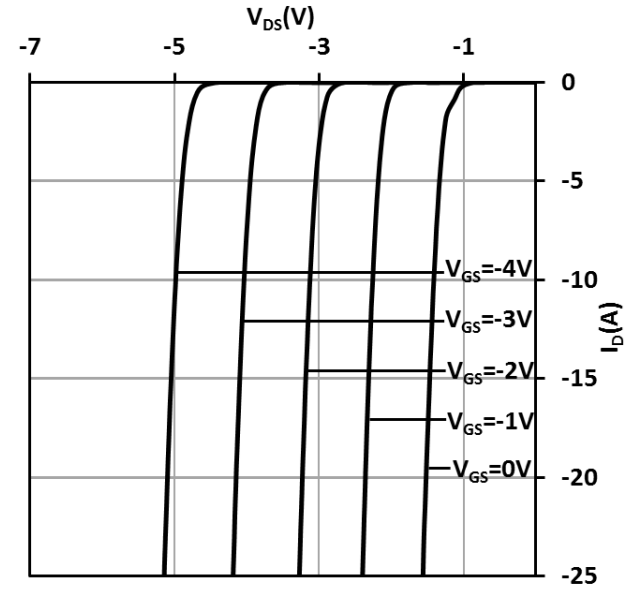


Figure 8 Typical Reverse Characteristics
($V_{GS}\geqslant 0, T_J$=25°C)

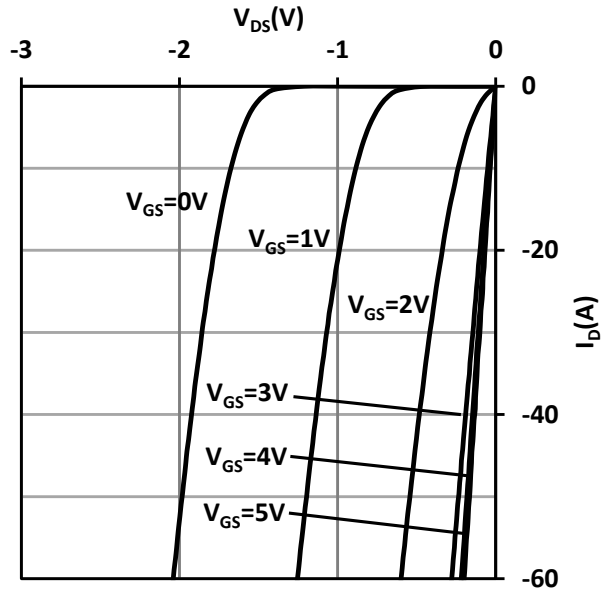


Figure 9 Typical Reverse Characteristics
($V_{GS}\leqslant 0, T_J=125°C$)

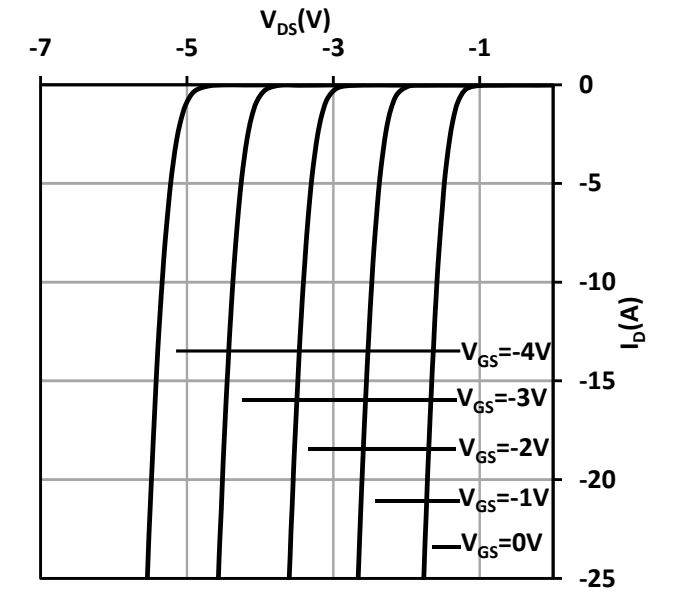


Figure 10 Typical Reverse Characteristics
($V_{GS}\geqslant 0, T_J=125°C$)

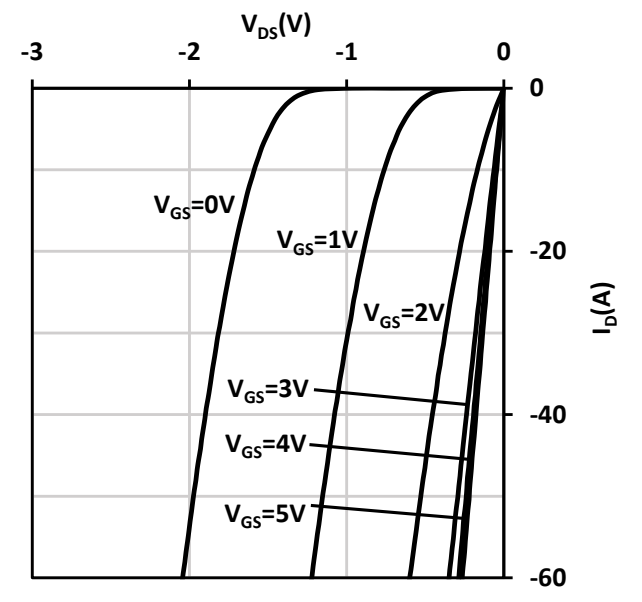


Figure 11 Typical Capacitances Characteristics

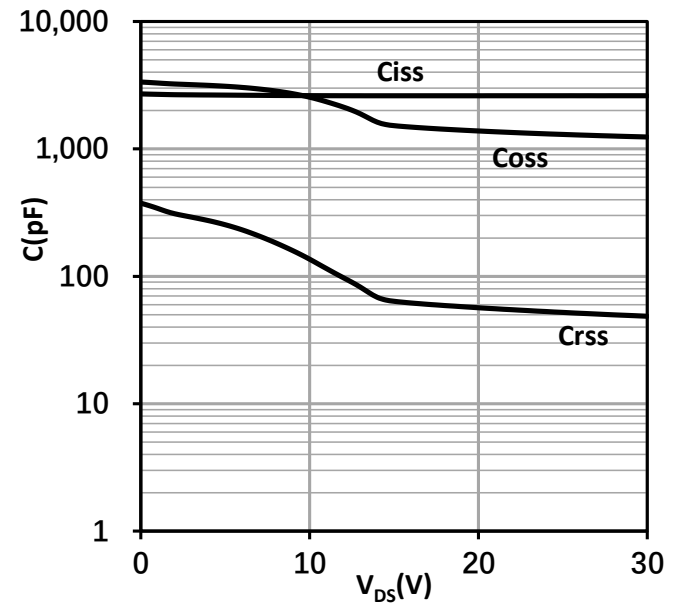


Figure 12 Typical Gate Charge

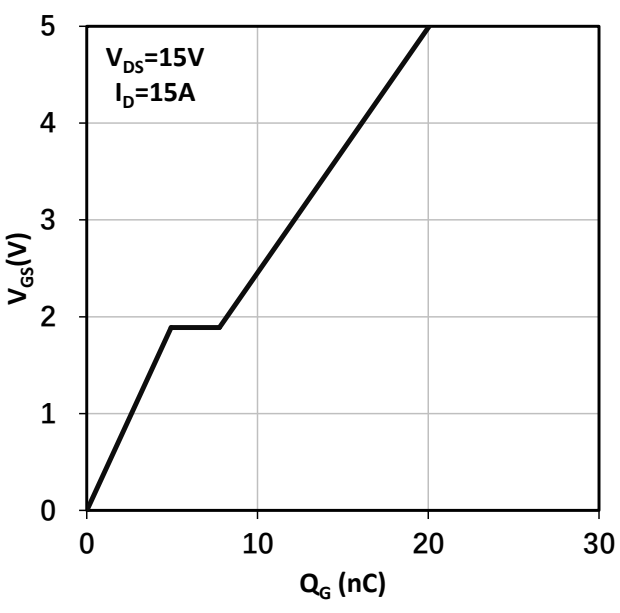


Figure 13 Normalized Threshold Voltage vs. Temp.

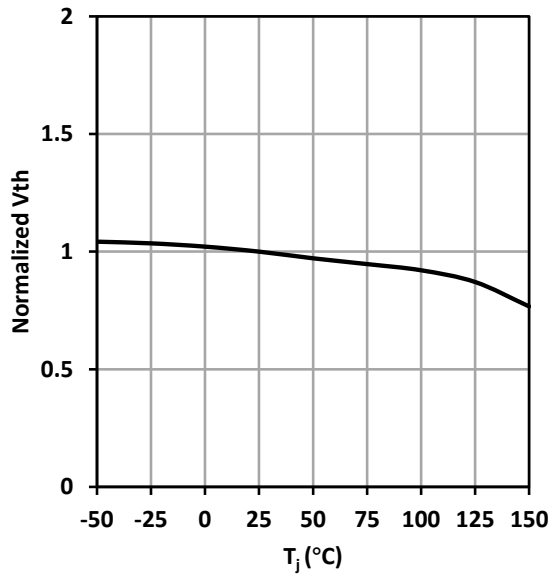


Figure 14 Output Charge

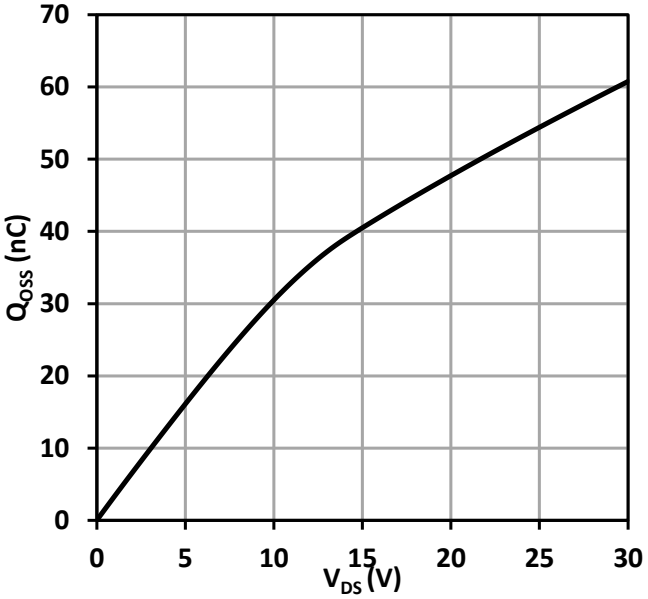


Figure 15 Output Capacitance Stored Energy

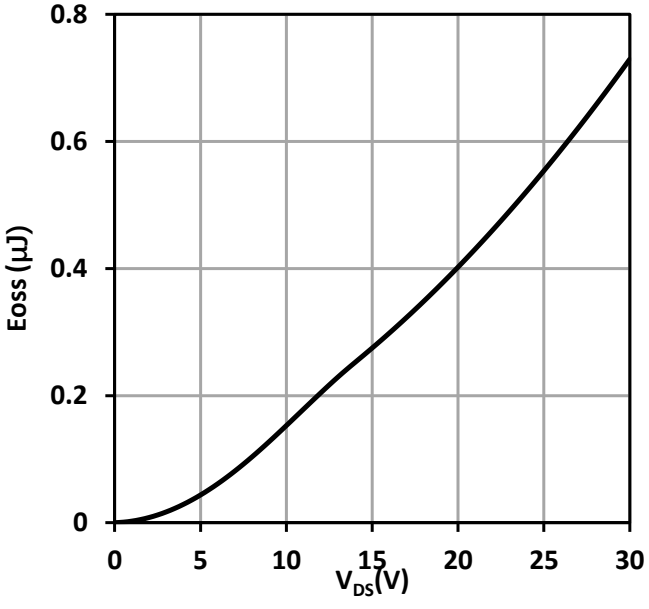


Figure 16 Power Dissipation

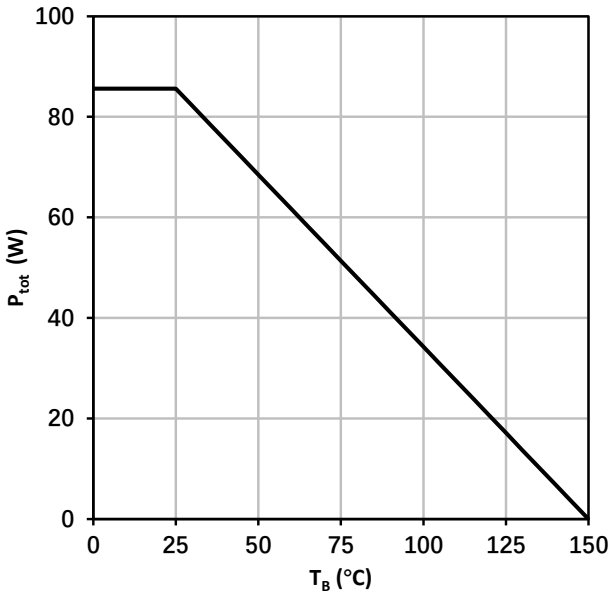


Figure 17 Safe Operating Area

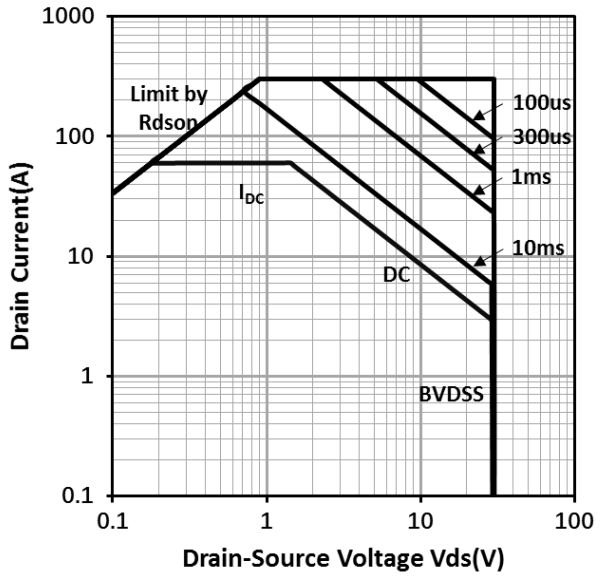
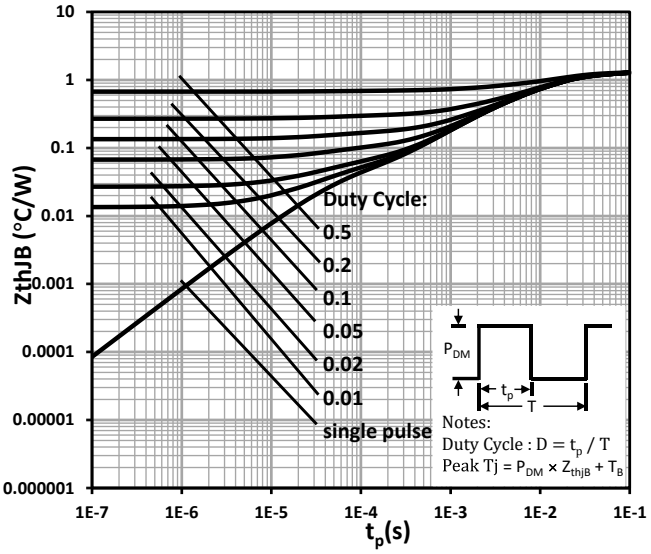
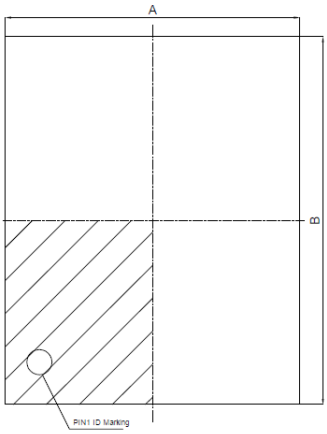


Figure 18 Max. Transient Thermal Impedance

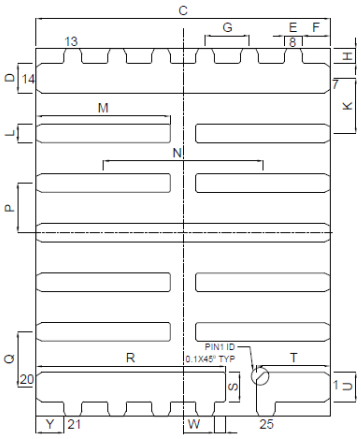


10. Package Outlines

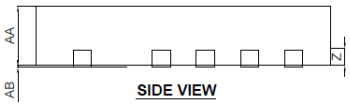
Package Reference



TOP VIEW



BOTTOM VIEW

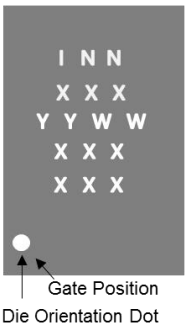


SIDE VIEW

NOTE:
1)ALL DIMENSION ARE IN MILLIMETERS.
2)BOTTOM VIEW IS FT TESTER SIDE VIEW.
3)LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4)COMPLIES WITH JEDEC MO-220.
5)DRAWING IS NOT TO SCALE.

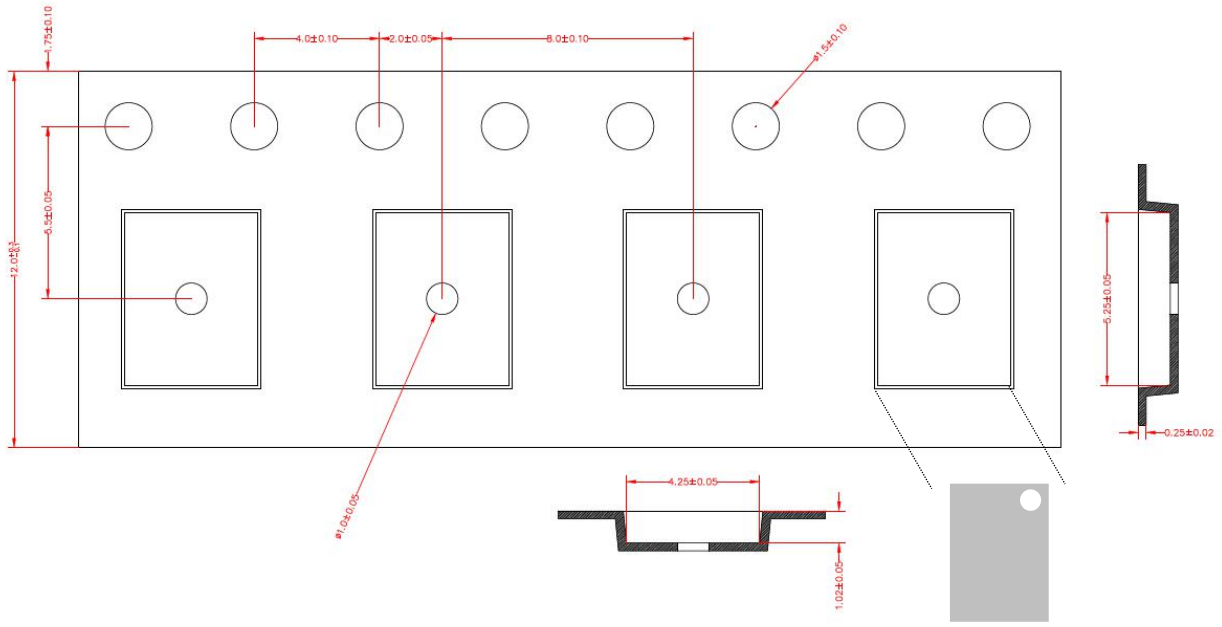
SYMBOL	MILLIMETER			NOTE
	MIN	NOM	MAX	
A	3.9	4.0	4.1	
B	4.9	5.0	5.1	
C	3.9	4.0	4.1	
D	0.350	0.400	0.450	
E	0.200	0.250	0.300	11X
F	0.375 REF			2X
G	0.600 BASIC			8X
H	0.200 REF			11X
K	0.750 BASIC			2X
L	0.200	0.250	0.300	10X
M	1.725	1.825	1.925	8X
N	2.175 BASIC			4X
P	0.675 BASIC			8X
Q	0.750 BASIC			2X
R	2.477	2.577	2.677	
S	0.350	0.400	0.450	
T	0.899	0.999	1.099	
U	0.350	0.400	0.450	
W	0.152 REF			
Y	0.375 BASIC			
Z	0.203 REF			
AA	0.650	0.750	0.850	
AB	0	0.02	0.05	

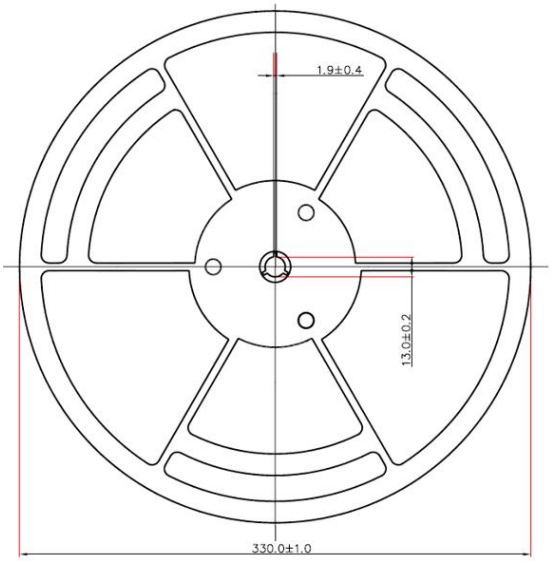
Marking Reference

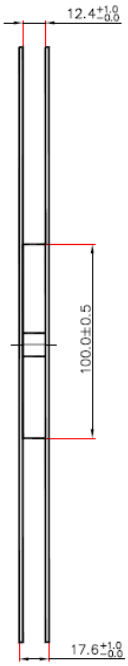


Row	Description	Example
Row 1	Company name	INN
Row 2	Product code	XXX
Row 3	Date code	YYWW
Row 4	Lot Code	XXX
Row 5		XXX

11. Reel Information



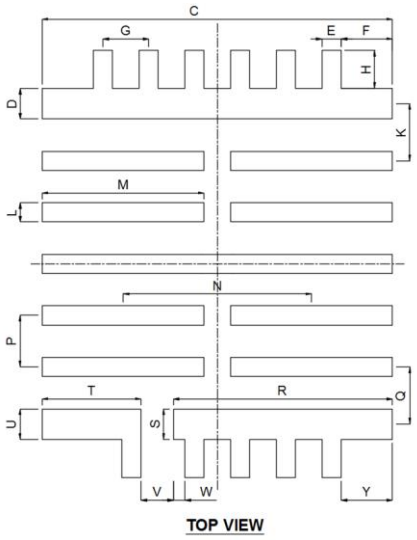




All dimension are in millimeters.

12. Land Pattern

Recommended Land Pattern



TOP VIEW

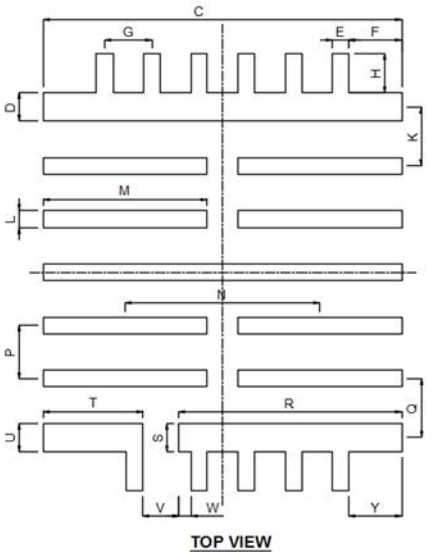
SYMBOL	MILLIMETER NOM	NOTE
C	4.600	
D	0.400	
E	0.250	11X
F	0.675	2X
G	0.600	8X
H	0.500	11X
K	0.750	2X
L	0.250	10X
M	2.125	8X
N	2.475	4X
P	0.675	8X
Q	0.750	2X
R	2.875	
S	0.400	
T	1.299	
U	0.400	
V	0.425	
W	0.152	
Y	0.675	

NOTE:

1) LAND PATTERN IS SOLDER MASK DEFINED.

2) IT IS RECOMMENDED TO HAVE ON-CU TRACE PCB VIAS.

Recommended Stencil Drawing



TOP VIEW

SYMBOL	MILLIMETER NOM	NOTE
C	4.560	
D	0.360	
E	0.210	11X
F	0.675	2X
G	0.600	8X
H	0.500	11X
K	0.750	2X
L	0.210	10X
M	2.085	8X
N	2.475	4X
P	0.675	8X
Q	0.750	2X
R	2.835	
S	0.360	
T	1.259	
U	0.360	
V	0.465	
W	0.152	
Y	0.675	

13. Revision History

Major changes since the last revision

Revision	Date	Description of changes
1.0	2023-12-27	1.0 Version Setup

Important Notice

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